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PATENT **Docket No. AUS920010547US2**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTORS:	**A.E. Mericas**	Examiner: J. West Art Unit: 2857
APPLICATION NO.	**10/733,443**	
FILED:	**December 10, 2003**	
TITLE:	**EXTENDING WIDTH OF PERFORMANCE MONITOR COUNTERS**	

CERTIFICATE OF MAIL

I hereby certify that this paper is being deposited with the U.S. Postal Service as First Class Mail, postage prepaid, in an envelope addressed to Commissioner for Patents, MAIL STOP APPEAL BRIEF-PATENTS, P.O. Box 1450, Alexandria, VA 22313-1450, Attention: Board of Patent Appeals and Interferences on January 17, 2006.

Lynn M. White

Commissioner for Patents
MAIL STOP APPEAL BRIEF-PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Attention: Board of Patent Appeals and Interferences

APPELLANTS' BRIEF

This brief is in furtherance of the Notice of Appeal filed in this case on November 10, 2005. It is submitted that this brief is in compliance with 37 CFR 41.37.

This brief is transmitted in triplicate. The Commissioner is authorized to charge the requisite fee ($500) set forth in §1.17(f) to Deposit Account No. 09-0447. Any additional required fees connected with this resubmission may be charged to Deposit Account No. 09-0447.

1. REAL PARTY IN INTEREST

The present application is assigned to International Business Machines Corporation, having its principal place of business at New Orchard Road, Armonk, New York 10504. Accordingly, International Business Machines Corporation is the real party in interest.

2. RELATED APPEALS AND INTERFERENCES

The appellant, assignee, and the legal representatives of both are aware of a pending appeal in related Application No. 09/931,308, of which the present application is a divisional, which may directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

3. STATUS OF CLAIMS

A. Claims canceled: 2 and 6

B. Claims withdrawn from consideration but not canceled: None

C. Claims pending: 1 and 3-5

D. Claims allowed: none

E. Claims rejected: 1 and 3-5

F. Claims appealed: 1 and 3-5

Appealed claims 1 and 3-5 as currently pending are attached as a Claims Appendix.

4. STATUS OF AMENDMENTS

A Reply under 37 C.F.R. §1.111 was filed on May 23, 2005 and resulted in the final Office Action appealed herein. An amendment after final was filed in the present case on September 16, 2005 to overcome issues under 35 U.S.C. §112. A Notice of Appeal was filed on November 10, 2005 and was received in the USPTO on November 14, 2005.

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

Claim 1: A performance monitor for monitoring an occurrence of incidences of one or more events related to operation of a processor, comprising: at least one monitor mode control register (*page 7, lines 10-11*); and a plurality of performance monitor counters operatively connected to said at least one monitor mode control register to count incidences of said one or more events (*page 7, lines 4-11*), said at least one monitor mode control register grouping said performance monitor counters so that when one of said performance monitor counters reaches capacity in connection with the counting incidences of a first of said one or more events, a second of said performance monitor counters begins counting subsequent incidences of said first of said one or more events (*page 7, lines 13-19)*; wherein the number of events equals X, and the number of performance monitor counters equals Y, whereby said at least one monitor mode control register groups said performance monitor counters into Z groups, wherein Y/X=Z; and wherein when X<Y, said at least one monitor mode control register assigns a number of performance monitor counters, said number of performance

monitor counters equal to an integer resulting from dividing Y by X, to each of said events to be counted; and wherein said at least one monitor control register assigns any unassigned performance monitor counters to at least one of said events (*page 7, line 4 through page 9, line 6*).

Claim 3: A performance monitor for monitoring an occurrence of incidences of one or more events related to operation of a processor, comprising: at least one control element (*page 7, lines 10-11*); and a plurality of counting elements operatively coupled to said at least one control element to count incidences of said one or more events (*page 7, lines 4-11*), said at least one control element grouping said plurality of counting elements so that when one of said plurality of counting elements reaches capacity in connection with the counting of incidences of a first of said one or more events, a second of said plurality of counting elements begins counting subsequent incidences of said first of said one or more events (*page 7, lines 13-19*); wherein the number of events equals X, and the number of counting elements equals Y, whereby said at least one control element groups said counting elements into Z groups, wherein Y/X=Z; and wherein when X<Y, said at least one control element assigns a number of counting elements, said number of counting elements equal to an integer resulting from dividing Y by X, to each of said events to be counted; and wherein said at least one control element assigns any unassigned counting elements to at least one of said events (*page 7, line 4 through page 9, line 6*).

The present invention is a performance monitor having plural counting elements (e.g., performance monitor counters or PMC's) and at least one control

element (e.g., a monitor mode control register or MMCR), where each counting element is controlled by the control element to pair or group the counting elements so that the overflow from one counting element can be directed to its pair/group. In a preferred embodiment of the present invention, when the number of events to be monitored is less than the number of counting elements, the control element groups the counting elements by dividing the number of available counting elements by the number of events being monitored by the counting elements; taking the integer portion of the result of this dividing step and assigning a number of counting elements, equal to that integer, to each of the events to be counted; and, if there are any remaining unassigned counting elements, assigning the unassigned counting elements to at least one of the events.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1 and 3-5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,557,548 to Gover et al. in view of U.S. Patent Application Publication No. 2002/0026524 to Dharap.

7. ARGUMENT - Rejection of Claims 1 and 3-5 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,557,548 to Gover et al. in view of U.S. Patent Application Publication No. 2002/0026524 to Dharap

A. Dharap is Non-Analogous Art with Respect to the Claimed Invention

Applicants respectfully traverse the rejection of the claims based on a proposed combination of Gover and Dharap as being an improper reliance on non-analogous art. The Dharap reference cited by the Examiner is in the field of cellular telephone displays and has nothing whatsoever to do with performance monitors and/or the division of PMCs among events being monitored by PMCs, and the Examiner has provided nothing in support of a contention that a person of ordinary skill in the field of PMCs would look to the field of cellular telephone displays to solve the problem of how to divide up the allocation of PMCs when the number of events to be monitored by the PMCs is less than the number of available PMCs.

Turning to the teachings contained in Dharap, Dharap is directed to a method for converting a list of data to a format suitable for display and manipulation in a limited display area (e.g., the display screen on a cellular phone). Dharap is classified for publication in U.S. Class 709, Subclass 236, which is for ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MULTICOMPUTER DATA TRANSFERRING, computer-to-computer protocol implementing, computer-to-computer data framing.

1) <u>The Examiner has not Met the Two-Part Deminski Test</u>

In In re Deminski, 796 F.2d 436, 230 U.S.P.Q. 313 (Fed.Cir. 1986) the Federal Circuit adopted a two-step test for determining whether particular references are within the appropriate scope of the art, and this test has been repeatedly relied upon to make this determination in subsequent cases. See, for example, In re Clay, 966 F2d. 656, 23 U.S.P.Q.2d 1058 (Fed.Cir. 1992); Wang Laboratories, Inc. v. Toshiba Corp., 993 F.2d 858, 26 U.S.P.Q.2d 1767 (Fed.Cir. 1993); and In re Oetiker, 977 F.2d. 1443 (Fed.Cir. 1992). See also MPEP 2141.01(a).

The two-part Deminski test requires that (1) a determination be made as to whether the reference is within the field of the inventor's endeavor, and (2), assuming the reference is outside that field, a determination be made as to whether the reference is reasonably pertinent to the particular problem with which the inventor was involved. In the present circumstances, neither test is met; thus, the references are not analogous art that can be combined to determine the patentability of the claims.

2) Dharap is Not Within the Field of the Inventors' Endeavor

Clearly, Dharap is not within the field of the inventor's endeavor herein. The subject invention is directed to performance monitors within a data processing system. Recognizing that interrupts could not be used during initial hardware testing of a processor in the data processing system, or when the processor was executing time-sensitive code, the inventor herein developed a novel performance monitor which increases the available width of PMCs during the initial hardware testing of the

processor or when the processor is executing time-sensitive code that cannot be interrupted.

Dharap has nothing to do with processor design, performance monitors, or extending the width of PMCs in a processor. The endeavor of Dharap is to enable the display of data on a small screen in a manner that is easy for a user of the small screen to use. This is clearly outside the field of endeavor of the inventor of the present invention.

3) Dharap is Not Reasonably Pertinent to the Particular Problem that the Inventor Solves

Since Dharap lies outside the field of the applicants' endeavor, the issue becomes whether the reference is reasonably pertinent to the particular problem with which the inventor was concerned. As noted above, the claimed invention is aimed at solving problems associated with the fact that interrupts could not be used during initial hardware testing of a processor in a data processing system, or when the processor was executing time-sensitive code. The applicant identified this problem and solved it by utilizing the present claimed structure.

A reference related to a displaying data on the small screen of a cellular telephone has no reasonable pertinence to solving the problem of an inability to use interrupts in certain situations involving hardware testing of a processor or the execution of time-sensitive code, problems that are solved by the present invention. One skilled in the art would not look to cellular telephone displays to solve such problems,

Furthermore, there is no reasonable basis for one skilled in the art attempting to solve an "interrupt problem" to turn to display screens of small hand-held devices in an attempt to solve such a problem. Display screens have nothing to do with interrupts; they merely display data that is useful to a user of the display screen.

Therefore, since Dharap is not reasonably pertinent to the interrupt problem, it is not analogous art according to the pertinent case law and MPEP 2141.01(a). Accordingly, the Dharap reference should be removed form consideration herein and the claims allowed.

B. The Cited Art Does Not Teach or Suggest the Claimed Invention

The Examiner has not Established a *prima facie* Case of Obviousness

As set forth in the MPEP:

> To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to modify the reference or to combine reference teachings.
> MPEP 2143

As noted above, the present invention is directed to a performance monitor that calculates the division of plural PMCs among events being monitored by the PMCs. U.S. Patent No. 5,557,548 to Gover et al. ("Gover") teaches a method and system which monitors specified events among the number of events within a data processing system. An MMCR allows control over which PMCs are used to monitor which events, and this control enables the ability of certain of the PMCs to be used for overflow of other PMCs. Applicant acknowledges that the present invention utilizes the control

concept taught by Gover. However, the present invention improves upon the functionality of Gover by providing structure that enables the MMCR to calculate the optimal division of the PMCs among the events being monitored, when there are fewer events than PMCs. This structure for performing division calculation is explicitly claimed in all of the independent claims, and thus is also claimed in all of the dependent claims.

The addition of Dharap does not teach the claimed elements, and does not provide a suggestion of a modification to achieve the claimed result. U.S. Patent Application Publication No. US 2002/0026524 to Dharap teaches, in the context of the limited ability to display data on the small screen of a wireless device, a method for converting a list of data to a format displayable on a limited display area. The list is sorted, grouped into sets, and then a set identifier is displayed which can be accessed by the user if they want more detail. For example, in an address list, instead of displaying McBurney, Michaels, Moorhead, etc., there is a single display of letters of the alphabet, and a user would select "M" to go into more detail if desired.

Of relevance to the present invention is the teaching in Dharap of granuralizing the list when the maximum number of available entry locations is less than the number of entries on the list. Dharap divides the total number of table entries by the number of available entries, and then displays an abbreviated list as a WAP page on a cellular phone. Dharap merely teaches that the display of data on a small display screen can be modified in a useable way to display less than the total of the data desired to be displayed, when needed. Since neither Dharap nor Gover teach or suggest the claimed

elements, it is submitted that the present invention patentably defines over Gover and Dharap, both alone and in combination. Accordingly, each of the independent claims, and all claims depending therefrom, patentably define over Gover and Dharap and are in condition for allowance.

The Board is respectfully requested to reconsider and withdraw the rejection of claims 1 and 3-5 under 35 U.S.C. §103.

8. CONCLUSION

For the foregoing reasons applicants respectfully request this Board to overrule the Examiner's rejections and allow claims 1 and 3-5.

Respectfully submitted:

JAN 17, 2006
Date

Mark D. Simpson, Reg. No. 32,942
Synnestvedt & Lechner LLP
2600 Aramark Tower
1101 Market Street
Philadelphia, PA 19107
Telephone: 215-923-4466
Facsimile: 215-923-2189

CLAIMS APPENDIX

CLAIMS INVOLVED IN THIS APPEAL:

1. (Previously presented) A performance monitor for monitoring an occurrence of incidences of one or more events related to operation of a processor, comprising:

at least one monitor mode control register; and

a plurality of performance monitor counters operatively connected to said at least one monitor mode control register to count incidences of said one or more events, said at least one monitor mode control register grouping said performance monitor counters so that when one of said performance monitor counters reaches capacity in connection with the counting incidences of a first of said one or more events, a second of said performance monitor counters begins counting subsequent incidences of said first of said one or more events;

wherein the number of events equals X, and the number of performance monitor counters equals Y, whereby said at least one monitor mode control register groups said performance monitor counters into Z groups, wherein Y/X=Z; and

wherein when X<Y, said at least one monitor mode control register assigns a number of performance monitor counters, said number of performance monitor counters equal to an integer resulting from dividing Y by X, to each of said events to be counted; and

wherein said at least one monitor control register assigns any unassigned performance monitor counters to at least one of said events.

2. (Canceled)

3. (Previously presented) A performance monitor for monitoring an occurrence of incidences of one or more events related to operation of a processor, comprising:

at least one control element; and

a plurality of counting elements operatively coupled to said at least one control element to count incidences of said one or more events, said at least one control element grouping said plurality of counting elements so that when one of said plurality of counting elements reaches capacity in connection with the counting of incidences of a first of said one or more events, a second of said plurality of counting elements begins counting subsequent incidences of said first of said one or more events;

wherein the number of events equals X, and the number of counting elements equals Y, whereby said at least one control element groups said counting elements into Z groups, wherein Y/X=Z; and

wherein when X<Y, said at least one control element assigns a number of counting elements, said number of counting elements equal to an integer resulting from dividing Y by X, to each of said events to be counted; and

wherein said at least one control element assigns any unassigned counting elements to at least one of said events.

4. (Original) The performance monitor as set forth in claim 3, wherein said at least one control element comprises a monitor mode control register.

5. (Previously presented) The performance monitor as set forth in claim 4, wherein each of said plurality of counting elements comprises a performance monitor counter operatively connected to said monitor mode control register.

6. (Canceled)

EVIDENCE APPENDIX

No further evidence is presented.

RELATED PROCEEDINGS APPENDIX

No related proceedings are presented.